Low Phase Noise S-band PLL Frequency Synthesizer Using DDS and Offset Mixing Techniques

Jaehung Choi #1, Minsu Kim #, Seungha Shin *, and Youngoo Yang #2

#School of Information and Communication Eng., Sungkyunkwan University., Suwon, 440-746, S. Korea
* cjh8783@skku.edu, yang09@skku.edu
# M&MLynx Corp., Yongin, 446-914, S. Korea

ABSTRACT—The paper presents the design and implementation of a DDS-driven PLL frequency synthesizer module using an offset mixing technique. The DDS, which is adopted as the reference generation for the PLL synthesizer, allows the synthesizer to have a fast switching time and narrow channel spacing. The offset mixing method allows an excellent in-band phase noise feature. The implemented frequency synthesizer has an excellent phase noise of -91.6dBc/Hz at an offset of 10KHz for the center frequency of 4.6GHz.

INDEX TERMS—Direct Digital Frequency Synthesizer, Frequency Synthesizer, Offset Mixing.

I. Introduction

A frequency synthesizer, which is one of the core building blocks for wired/wireless telecommunication systems or radar systems, generates a high-frequency carrier using a reference clock. In addition, it is a very critical block that significantly affects the signal purity in telecommunication systems.

Table 1

<table>
<thead>
<tr>
<th>Direct vs. Indirect Frequency Synthesizers</th>
<th>DFS</th>
<th>IFS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching time</td>
<td>Fast</td>
<td>Slow</td>
</tr>
<tr>
<td>Phase noise</td>
<td>Good</td>
<td>Normal</td>
</tr>
<tr>
<td>Circuit</td>
<td>Complex</td>
<td>Simple</td>
</tr>
<tr>
<td>Spurious</td>
<td>Bad</td>
<td>Good</td>
</tr>
</tbody>
</table>

DFS: Direct Frequency Synthesizer
IFS: Indirect Frequency Synthesizer

There are two frequency synthesis techniques, namely, the direct and indirect synthesis methods. The direct frequency synthesis method has merits of fast frequency switching time and low phase noise and demerits of being quite complex and generating spurious signals.

In contrast, the indirect frequency synthesis method has advantages of generating less spurious signals, having simple architecture, and being capable of reducing the phase noise by using a feedback loop, however, it has a relatively long switching time [1]-[2]. Table 1 summarizes the general features of the direct and indirect frequency synthesizers.

In this paper, a PLL frequency synthesizer, which operates in the frequency band of 3.7~4.7GHz, has been designed and implemented using the indirect frequency synthesis method. The synthesizer includes the reference clock generation, based on DDS, for high-speed frequency switching and narrow channel spacing, as well as the offset mixing method for low in-band phase noise characteristics.

In section II, the DDS method, which is adopted to generate the reference clock to the PLL, is described as well as the simulation results for the in-band phase noise characteristics, from using the offset mixing method. In section III, the operation and architecture of the proposed frequency synthesizer is presented and finally, the experimental results and conclusions are given in section IV.

II. DDS and Offset Mixing Methods

A. DDS (Direct Digital Frequency Synthesizer)

The DDS system comprises a phase accumulator, an amplitude/sine converter and a D/A Converter, as shown in Fig. 1. The DDS circuit includes a look-up table, which has the phases and amplitudes of the sine wave of the required frequency, which is directly reproduced according to the phase and amplitude values in the look-up table [3].

Since the n-bit frequency tuning word (FTW) must be supplied by an external controller, the reference clock is sampled to give 2n samples so that the frequency resolution of the DDS is as follows:

\[ F_{out} = \frac{M \times F_{ref}}{2^n} \]

where \( F_{out} \) and \( F_{ref} \) are the frequencies of the output signal and internal reference clock, respectively; and \( M \) and \( n \) are the binary tuning word and the bit number of the phase accumulator, respectively. As shown in (1), the frequency resolution can be enhanced by increasing the number of
However, for general DDS systems, unnecessary frequency components, such as harmonics, spurious tones, and power line noise effects, are easily generated in the output signals. Therefore, in this paper, a Chebyshev-type low pass filter has been designed and added to the output of the DDS circuit and Fig. 2 shows the circuit diagram and output responses of the designed LPF.

\[\text{Fig. 2. Circuit diagram and output responses of the LPF at the output of the DDS circuit}\]

B. Direct Offset Mixing

Generally, the in-band phase noise of frequency synthesizers can be lowered by reducing the N-divider value in the PLLs [5] and Fig. 3 shows the simulated phase noise characteristics using ADI’s SimPLL for the N-divider ratios of 223 and 300. It is clearly seen that the in-band phase noise can be reduced by up to 4.5dB as the N-divider is reduced. The offset-mixing method is used to reduce the number of the N-division so that the phase noise performance of the PLL synthesizer can be improved accordingly. The indirect frequency synthesizer is based on a feedback system, i.e. the PLL, which consists of a phase frequency detector (PFD), a loop filter, a frequency divider and a VCO. The PLL controls the output frequency while also controlling the frequency division ratio at the feedback loop. Fig. 4 illustrates the block diagram of the PLL frequency synthesizer using DDS and the offset mixing methods.

\[\text{Fig. 3. Phase noise characteristics according to the dividing number}\]

III. Design and Implementation

The signal, generated by the DDS, has a very stable frequency and low phase noise, and is applied to the phase frequency detector of the PLL as a reference signal. Subsequently, the reference signal is compared for its phase with the output signal, which is down-converted, and divided by the offset mixing and the divider circuits, respectively. The phase difference between two signal inputs of the PFD generates the control voltage for the VCO through the charge pump and the loop filter. The loop filter removes any high frequency components in the output voltage of the phase detector, and determines the loop bandwidth of the whole PLL.

Additionally, the offset mixing method, using a mixer, is employed in the proposed system in order to reduce the division ratio of the N-divider. The signal, down--converted by the mixer, passes the BPF, is divided by N-divider, and is compared with the reference frequency from the DDS. For the DDS system, Analog Device’s AD 9910, has been used which enables an adjustment of the channel spacing down to a few KHz as the output frequency and PLL itself are controlled; in addition, Analog Device’s ADF4106 has been deployed for the integer-N PLL IC. The loop filter, which
determines the bandwidth of the PLL system, has been designed as a third-order active filter whose schematic diagram is shown in Fig. 6; its bandwidth in this design is 250KHz.

The LO signal in the offset mixing circuit has a frequency of 1,200MHz and a power level of 7dBm so that the synthesizer can reduce the N value of the divider to 77. All the circuits are implemented on a PCB, based on the FR4 and the PCB area for the DDS and PLL should be carefully isolated to reject various noise effects, including the power line noise.

IV. Experimental results

For the last block of the frequency synthesizer, Synergy Microwave’s DCYS-300600-5 has been used as a VCO with a frequency tuning range of 3–6GHz. For the offset mixing method, Pulsar Microwave’s passive mixer, XL-10-A, has been adopted due to its high linearity characteristics. Fig. 5 shows a photograph of the implemented PLL frequency synthesizer and Table 2 shows the components used in the implementation of the PLL frequency synthesizer.

<table>
<thead>
<tr>
<th>Part</th>
<th>Part number</th>
<th>Company</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS</td>
<td>AD9910</td>
<td>Analog Devices</td>
</tr>
<tr>
<td>PLL</td>
<td>ADF4106</td>
<td>Analog Devices</td>
</tr>
<tr>
<td>VCO</td>
<td>DCYS-300600-5</td>
<td>Synergy</td>
</tr>
<tr>
<td>MIXER</td>
<td>XL-10-A</td>
<td>Pulsar microwave</td>
</tr>
<tr>
<td>PCB</td>
<td>FR-4</td>
<td>-</td>
</tr>
</tbody>
</table>

| Table 2: Implementation details of the PLL frequency synthesizer module |

Fig. 7 shows the measured output spectra of the DDS before and after filtering and Fig. 8 presents the measured frequency tuning range of the VCO according to the control voltage variation. The VCO can be tuned for the wide frequency range from 3.7 to 4.7GHz.

Fig. 9 shows the output spectrum of the implemented frequency synthesizer module where it can be seen in the measured results that there are no large spurious signals since the LPF, after the DDS has been included.

Fig. 10 presents the measured phase noise characteristics at the carrier frequency of 4.67GHz where the measured phase noise performances are -91, -84, -109dBc/Hz at frequency offsets of 10, 100, and 1,000KHz, respectively.

In comparison to Table 3, the proposed frequency synthesizer shows very good phase noise performance by virtue of the combined use of the DDS and the offset mixing method.
Fig. 8. The measured frequency tuning range of the VCO

Fig. 9. The measured output frequency spectrum of the implemented frequency synthesizer

Fig. 10. The measured output phase noise

Table 3
Comparison with previously published results.

<table>
<thead>
<tr>
<th>Type</th>
<th>Frequency</th>
<th>Phase noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS Driven</td>
<td>1.712 GHz</td>
<td>80.3dBc/Hz @1KHz</td>
</tr>
<tr>
<td>DDS Driven</td>
<td>8.4GHz</td>
<td>87.43dBc/Hz @10KHz</td>
</tr>
<tr>
<td>PLL(Crystal Reference)</td>
<td>2.82GHz</td>
<td>94.3dBc/Hz @10KHz</td>
</tr>
<tr>
<td>DDS+Offset Mixing</td>
<td>4.7GHz</td>
<td>91.6dBc/Hz @10KHz</td>
</tr>
</tbody>
</table>

method. In addition, the implemented synthesizer has a very narrow channel spacing that is as narrow as a few KHz because of the DDS method used.

V. Conclusions

In this paper, a PLL frequency synthesizer module, which has excellent performances in the frequency range of 3.7~4.7GHz, has been designed and implemented using the DDS-driven reference generation, and offset mixing methods. The DDS-driven reference generation method allows fast switching time and precise channel spacing, while the offset mixing method allows very good in-band phase noise characteristics.

The implemented PLL frequency synthesizer module has shown good performance, with an excellent phase noise of about -91.6dBc/Hz at a frequency offset of 10KHz over the wide frequency band of 3.7~4.7GHz. It also has very narrow channel spacing of a few KHz compared to the conventional PLL frequency synthesizers.

REFERENCES