High-Power Inverted Doherty Power Amplifier for Broadband Application

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Abstract
This paper presents a high-power inverted Doherty power amplifier for broader operational bandwidth. After analyzing two operation modes according to the load modulation of the Doherty power amplifier, the inverted Doherty structure was selected. In the design, the load impedances for optimum broadband characteristics at both the back-off and peak power levels. The Doherty power amplifier was designed to have simultaneously optimized back-off efficiency and load impedances at peak power level. The designed inverted Doherty power amplifier based on LDMOSFET’s shows high efficiency of more than 40 % at the point backed-off by 6 dB from the 1 dB compression point of 50 dBm and at the band from 2.04 to 2.24 GHz.

Keyword: Doherty power amplifier, inverted Doherty power amplifier, broadband Doherty power amplifier, high-power amplifier.

1. Introduction
Modern wireless communication systems, such as WiMAX, W-CDMA, and LTE, have modulated signals that have high peak-to-average power ratio (PAPR). Therefore, power amplifiers (PA) operate at backed-off region from the peak power in order to comply with the linearity specifications, which causes efficiency degradation.

The Doherty power amplifiers (DPA’s) takes advantage in back-off efficiency of load modulation using a quarter-wave line [1]. The DPA’s have been widely used due to their simple circuits and superior performances. However, DPA’s have limited bandwidth for high-efficiency operation mainly because of the load impedance modulation using the quarter-wave line.

Various studies have been carried out to broaden the bandwidth of DPA’s. In [2], the matching networks follow optimum impedances at each frequency point by using a real-frequency technique. In [3], based on an analysis for the load modulation, new-type of the output combiner was proposed for broadband characteristics.

The ratio of impedance transformation reduced to 1:2.85 from 1:4, so that the frequency effect on the impedance transformation can also be reduced in [4]. After resonating the parasitic capacitance in the device out, the matching network can be designed only using a resistive load in [5]. In [6], the optimum impedance at back-off according the frequency become less sensitive using a newly shaped output combiner. However, high-power broadband DPA’s are very difficult to design because of low load impedance of the transistor.

In this paper, we designed high-power broadband inverted Doherty power amplifier (IDPA) with an output power of more than 100 W. Optimum load impedances over the frequency band were extracted. The optimum reference impedance was found for the various load conditions. The IDPA was designed with considering the optimum load impedances at the
both back-off power and peak power. No quarter-wave line in the carrier PA due to the IDPA structure, the output combiner becomes more insensitive over frequency. The design procedure and simulation results of the IDPA using high-power LDMOSFET’s will be presented.

2. Broadband IDPA

For the conventional Doherty power amplifiers (CDPA’s), there is a quarter-wave transformer, whose characteristic impedance of $R_s$, at the carrier PA to transform $R_0$ to $R_0/2$. Generally between the load and the junction that combines current from the carrier and peaking PA’s, there is another quarter-wave line. Two quarter-wave lines limit the bandwidth of the CDPA.

Especially at back-off power level, triple impedance transformation happens due to the two quarter-wave lines and the load matching network of the carrier PA. This can cause significant performance degradation at back-off power level according to the frequency variation. For broadband characteristics, it is required to reduce the performance degradation at back-off power level.

Figure 1 presents the output combining circuit of the IDPA. For the IDPA structure, there is no quarter-wave line after the carrier PA for load modulation. At back-off power level when the peaking PA is off, impedance transformation occurs only twice due to the quarter-wave line of $R_T$ and the load matching network of the carrier PA. Thus, output combiner of the IDPA shows less sensitive characteristics over frequency variation compared to the CDPA.
Figure 2 shows schematic diagrams of the IDPA load networks for two operation modes. $Z_{opt,L}$ and $Z_{opt,H}$ are optimum impedances at back-off and peak power levels, respectively. For the back-off power level, as shown in Figure 2 (a), peaking PA is off and the load impedance after a quarter-wave line of $R_T$ is $R_{L,L}$. The carrier and peaking PA’s drive the same current at the peak power level as the peaking PA is full turned on, as shown in Figure 2 (b). Therefore, the carrier and peaking PA’s see the same impedance of $R_{L,H} (=2R_{L,L})$ at the peak power level.

For broadband operation, it is important for the transistors to have load impedance near the optimum for the overall operating frequency band. Figure 3 shows the matching network and impedances of the carrier PA. Since the carrier PA operates with two modes, it required to have two different optimum load conditions of $Z_{opt,L}$ and $Z_{opt,H}$ for the back-off and peak power levels, respectively.

In addition, $R_{L,L}$ which is selected by the characteristic impedance of the quarter-wave line after the combining junction affects the bandwidth of the matching network as well. For good and broad back-off performance, the matching network is optimized for $Z_{opt,L}$. At the peak power level, the load impedance is transformed from $2R_{L,L}$ to around $Z_{opt,H}$ by the matching network and offset line which has a characteristic impedance of $R_{L,L}$.
Fig. 4: Optimum impedances and load impedances of the matching network for various $R_{L,L}$ at the band from 2.04 to 2.24 GHz: (a) at the back-off power level, (b) at the peak power level.

Figure 4 represents the optimum impedances and simulated load impedances of the matching network for various $R_{L,L}$: (a) at the back-off power level and (b) at the peak power level. The optimum impedances were extracted using load-pull simulation over the frequency band of 2.04 to 2.24 GHz with a step of 50 MHz. When $R_{L,L} = 25\Omega$, the simulated load impedances are closest to the optimum impedances.

![Diagram](image)

Fig. 5: Peaking PA design: (a) schematic and impedances, (b) output reflection coefficient after the matching network and offset line at the band from 2.04 to 2.24 GHz.
Figure 5(a) shows the schematic and impedances of the peaking PA. It has a quarter-wave line after the matching network and offset line. The output reflection coefficient after the matching network and a proper matching network is near to the short point on the Smith chart, as shown in Figure 5(b). Therefore, it requires a quarter-wave line to transform the output reflection coefficient to the open point, so that the IDPA configuration is accomplished.

Figure 5: Schematic and impedances of the peaking PA.

Fig. 6: Schematic diagram of the designed broadband IDPA.

Figure 6 is a schematic diagram of the designed broadband IDPA. The circuit was designed using Agilent’s Advanced Design System (ADS). Freescale’s 190-Watt push-pull LDMOSFET (MRF6P21190H) was used. For the gain balance between the carrier PA and peaking PA, an 1dB attenuator is employed at the input of the carrier PA. A delay compensation line is inserted in the input stage of the carrier PA.

3. Results

![Graph showing Gain (dB) and PAE (%) vs. Output power (dBm)]
Fig. 7: Simulated gain and PAE of the designed IDPA using a 1-tone input with a frequency of 2.14 GHz.

![Figure 7: Simulated gain and PAE of the designed IDPA using a 1-tone input with a frequency of 2.14 GHz.](image)

**Figure 7** shows simulation results for the designed IDPA using a 1-tone signal with a frequency of 1 GHz. The IDPA has a P1dB of 52.77 dBm and a PAE of 51.53% at the 6dB back-off point from P1dB. Figure 8(a) presents simulated gains and P1dB’s of the CDPA and the IDPA over the frequency band from 2.04 to 2.24 GHz. Figure 8(b) shows the PAEs at the peak power and 6dB back-off power levels at the operating frequency band. The designed IDPA has P1dB of more than 50 dBm and back-off PAE of more than 40%. The designed IDPA clearly has broader bandwidth and better performances than that of the CDPA. Table 1 summarizes the performances of the previously published works regarding broadband DPA.
Table 1: Comparison to the previous results for the broadband DPA

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Output power (dBm)</th>
<th>5-6 dB back-off efficiency</th>
<th>Freq. range (GHz)</th>
<th>Device</th>
</tr>
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<tbody>
<tr>
<td>[2]</td>
<td>41</td>
<td>40 %*</td>
<td>2.2 – 2.96</td>
<td>GaN</td>
</tr>
<tr>
<td>[3]</td>
<td>49</td>
<td>50 %*</td>
<td>0.7 – 1</td>
<td>GaN</td>
</tr>
<tr>
<td>[4]</td>
<td>42</td>
<td>41 %**</td>
<td>1.7 – 2.6</td>
<td>GaN</td>
</tr>
<tr>
<td>[5]</td>
<td>42</td>
<td>40 %*</td>
<td>1.7 – 2.1</td>
<td>LDMOS</td>
</tr>
<tr>
<td>[6]</td>
<td>42</td>
<td>48 %*</td>
<td>1.95 – 2.25</td>
<td>GaN</td>
</tr>
<tr>
<td>[8]</td>
<td>37</td>
<td>31 %**</td>
<td>1.5 – 2.14</td>
<td>GaN</td>
</tr>
<tr>
<td>This work</td>
<td>50</td>
<td>40 %**</td>
<td>2.04 – 2.24</td>
<td>LDMOS</td>
</tr>
</tbody>
</table>

* Drain efficiency
** Power added efficiency

4. Conclusions

In this paper, based on the analysis for the two operating modes of DPA, a broadband IDPA is proposed. The IDPA structure allows the output combiner to be less sensitive to the frequency changes because there is no quarter-wave line after the carrier PA. The optimum load impedances were extracted using a load-pull simulation for both the back-off and peak power levels over the operating frequency band. The matching network was designed to simultaneously provide load impedances close to the optimum impedances at the back-off and peak power levels. The IDPA was designed using a 190-Watt push-pull LDMOSFET. At the 200MHz band from 2.04 to 2.24 GHz, it has P1dB of more than 50 dBm and efficiency at 6 dB back-off of more than 40%.

5. References